CLAIMS

Having thus described the invention in detail, what we claim is new, and desire to secure by Letters Patent is:

1. A method for forming a low resistance MOSFET device comprising the steps of:

forming a gate region atop a surface of a substrate;

forming first spacers having a first spacer width on sidewalls of said gate region;

forming first silicide regions having a first silicide thickness in said substrate as well as atop a surface of said gate region;

forming second spacers having a second width greater than said first spacer width on said substrate, wherein said second spacers protect said first silicide region in said substrate; and

forming second silicide regions in said substrate and atop a surface of said gate region, wherein said second silicide regions have a thickness that is greater than said first silicide thickness

2. The method of Claim 1 wherein said forming of said gate region further comprises predoping of said gate region.

3. The method of Claim 2 wherein said predoping is performed by ion implantation of a type III-A element or a type V element into said gate region.

4. The method of Claim 3 where predoping is achieved via ion implantation of phosphorus into said gate region.

5. The method of Claim 1 further comprising the step of forming source/drain extension regions following said gate region formation.

6. The method of Claim 1 wherein said first spacer width is from about 5 nm to about 20 nm.

7. The method of Claim 1 wherein said first spacer width is from about 7 nm to about 15 nm.

8. The method of Claim 1 wherein said second spacers width is from about 20 nm to about 90 nm.

9. The method of Claim 1 wherein said second spacers width is from about 30 nm to about 70 nm.

10. The method of Claim 1 further comprising the steps of forming deep source/drain regions after forming said first spacers.

11. The method of Claim 10 wherein forming said deep source/drain regions comprises ion implantation of a type III-A element or a type V element into said substrate.

12. The method of Claim 1 wherein said forming of said first silicide region comprises depositing a first metal layer upon an exposed surface of said substrate and annealing.

13. The method of Claim 12 where said first metal layer has a thickness from about 2 nm to about 7 nm.

14. The method of Claim 13 where said first metal layer comprises Ta, Ti, W, Pt, Co, Ni, or combinations thereof.

15. The method of Claim 1 wherein said first silicide regions have a thickness of about 1 nm to about 20 nm.

16. The method of Claim 1 wherein said first silicide regions have a thickness from about 2 nm to about 15 nm.

17. The method of Claim 1 wherein said first silicide regions have a thickness from about 5 nm to about 12 nm

18. The method of Claim 1 wherein said first silicide region is formed in said substrate having a channel region beneath said gate region, where the distance between said silicide region and said channel region is from about 2 nm to about 15 nm.

19. The method of Claim 1 wherein said first silicide region is formed in said substrate having a channel region beneath said gate region, where the distance between said silicide region and said channel region is from about 3 nm to about 10 nm.

20. A low resistance MOSFET device comprising: a substrate having a first silicide region with a first silicide thickness and abutting a second silicide region with a second silicide thickness, wherein said second silicide thickness is greater than said first silicide thickness; a patterned gate region atop said substrate; first spacers abutting sidewalls of said pattern gate region having a first spacer width; and second spacers abutting sidewalls of said first spacers having a second spacer width that is greater than said first spacer width, wherein said second spacers are positioned atop and self aligned to said first silicide region.

21. The low resistance MOSFET of Claim 20 further comprising source/drain extension regions and a channel region, where said source/drain extension regions are positioned between said first silicide region and said channel region, where a

dimension between said channel region and said source/drain extension regions is from about 2 nm to about 15 nm.

22. The low resistance MOSFET of Claim 20 further comprising source/drain extension regions and a channel region, where said source/drain extension regions are positioned between said first silicide region and said channel region, where a dimension between said channel region and said source/drain extension regions is from about 3 nm to about 10 nm.

23. The low resistance MOSFET of Claim 20 further comprising source/drain extension regions and a channel region, where said source/drain extension regions are positioned between said first silicide region and said channel region, where dimension between said channel region and said source/drain extension regions is about 7 nm.

24. The low resistance MOSFET of Claim 20 wherein said first spacer width is from about 3 nm to about 40 nm.

25. The low resistance MOSFET of Claim 20 wherein said first spacer width is from about 5 nm to about 20 nm.

26. The low resistance MOSFET of Claim 20 wherein said first spacer width is from about 7 nm to about 15 nm.

27. The low resistance MOSFET of Claim 20 wherein said second spacer width is from about 20 nm to about 90 nm.

28. The low resistance MOSFET of Claim 20 wherein said second spacer width is from about 30 nm to about 70 nm.

29. The low resistance MOSFET of Claim 20 wherein said first silicide region has a thickness of approximately 1 nm to about 20 nm.

30. The low resistance MOSFET of Claim 20 wherein said first silicide region has a thickness of approximately 2 nm to about 15 nm.

31. The low resistance MOSFET of Claim 20 wherein said first silicide region has a thickness of approximately 5 nm to about 12 nm.

32. The low resistance MOSFET of Claim 20 wherein said second silicide region has a thickness of about 10 nm to about 40 nm.

33. The low resistance MOSFET of Claim 20 wherein said second silicide region has a thickness of about 15 nm to about 35 nm.